Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A dynamic random access memory (DRAM) having a refresh-control function under control by an internal refresh-control signal comprising:

a cell array having a plurality of DRAM cells divided into a plurality of blocks, the DRAM cells being driven through word lines for data transfer with bit lines;

a decoder to select word lines and bit lines connected to the cell array;

a sense amplifier to amplify data on the bit lines; and

a refresh controller to limit refresh to the cell array so that at least one externally-accessed block cell among the blocks is refreshed[[.]];

wherein the refresh controller comprises:

a refresh counter to generate an internal address signal, the address being increased for each refresh to the cell array;

a register, provided per block of the cell array, the register storing information indicating whether each block has been accessed;

a refresh limiter to halt refresh to each block that has not been accessed; and

a refresh-restriction releasing section that is data programmable for releasing the refresh limiter from refresh limit to the cell array.

2. (Canceled)

3. (Currently Amended) The DRAM according to claim ~~2~~ 1, wherein the register stores information indicating whether there is a write access to each block.

4. (Currently Amended) The DRAM according to claim ~~2~~ 1 further comprising an external rest terminal through which the information stored in the register is initialized per block of the cell array.

5. (Original) The DRAM according to claim ~~2~~ 1 further comprising a reset circuit to initialize the information stored in the register.

6. (Canceled)

7. (Currently Amended) The DRAM according to claim ~~6~~ 1, wherein the refresh-restriction releasing section includes a fuse circuit.

8. (Currently Amended) The DRAM according to claim ~~6~~ 1, wherein the refresh-restriction releasing section includes a bonding option.

9. (Original) The DRAM according to claim ~~6~~ 1 further comprising an access detector to detect an external access to the cell array, the refresh-restriction releasing section generating a first operation-halt signal to deactivate the access detector to release the cell array from refresh limit.

10. (Original) The DRAM according to claim 9, wherein the refresh-restriction releasing section generates a second operation-halt signal to deactivate the refresh limiter to release the cell array from refresh limit.

11. (Original) The DRAM according to claim 10, wherein the refresh-restriction releasing section generates a third operation-halt signal to deactivate the register, thus deactivating all of the access detector, the refresh limiter and the register to release the cell array from refresh limit.

12. (Original) The DRAM according to claim 9, wherein the refresh-restriction releasing section generates only the first operation-halt signal to the access detector while the refresh limiter is active, with the register being set at non-active, to release the cell array from refresh limit.

13. (Original) The DRAM according to claim ~~6~~ 1, wherein the refresh-restriction releasing section generates a second operation-halt signal to the refresh limiter for deactivating the refresh ~~limitter~~ limiter, to release the cell array from refresh limit.

14-17. (Canceled)

18. (Original) A dynamic random access memory (DRAM) having a refresh-control function under control by an internal refresh-control signal comprising:

a cell array having a plurality of DRAM cells divided into a plurality of blocks, the DRAM cells being driven through word lines for data transfer with bit lines;

a decoder to select word lines and bit lines;

a sense amplifier to amplify data on the bit lines;

a refresh counter to generate an internal address signal, the address being increased for each refresh to the cell array;

a register, provided per block of the cell array, the register storing information indicating whether each block has been accessed;

a refresh limiter to halt refresh to each block that has not been accessed; and

a refresh-restriction releasing section that is data programmable for releasing the refresh limiter from refresh limit to the cell array.

19. (Original) The DRAM according to claim 18, wherein the refresh-restriction releasing section includes a fuse circuit.

20. (Original) The DRAM according to claim 18, wherein the refresh-restriction releasing section includes a bonding option.